29. 11.

Review of the Doctoral Thesis
Implementation Methods of LD-RLS with Directional Forgetting for Embedded Systems on a Chip
submitted by Ing. Roman Bartosiński

a) ***Is the treated topic up to date?***

Submitted thesis deals with the implementation of rather specific algorithms: recursive least squares based on LDU decomposition (LD-RLS) with directional forgetting. These algorithms belong to those adaptive algorithms seldom implemented today, mainly due to their computational complexity. As current embedded platforms are providing sufficient performance, implementation of such adaptive algorithms becomes feasible and tends towards very efficient – Systems on a Chip (SoC) or even more complex Network on Chip (NoC). Since the SoC/NoC are of high practical importance for robotics, implementation of sensing and artificial intelligence, it is no doubt that the treated topic is most up to date.

b) ***What methods have been selected?***

The goal of the thesis is to implement highly sophisticated algorithms into existing real embedded platform. Beside the theoretical background, author proofs its orientation in the real environment – in terms of the knowledge of recent technologies so as in terms of its deployment. I appreciate author's participation in couple of national/European research projects (p. i).

Next to the discursive theoretical background review presented within Chapter 2 and 3 he has chosen two RLS algorithms for embedded implementation. In this sense, particular practical consequences of exponential forgetting EF LD-RLS in comparison with directional forgetting DF LD-RLS algorithms might be more highlighted (p. 8).

The selected algorithms have been implemented onto two embedded platforms: on the systolic array and on the UTIA DSP platform utilizing FPGA technology. In this sense I consider the thesis results as very high quality results. UTIA DSP platform (p. 62) is recognized and widely used as accelerator for SoC and its extension is of high importance.

The implementation of selected adaptive algorithms is followed by presentation of several test cases for system identification and for slow and fast parameter tracking. In order to ensure that algorithms with different forgetting methods are certainly comparable, specific new assessment method has been proposed.

c) ***Did the thesis succeed to achieve its goal?***

Based on a comprehensive theoretical background of the author, the thesis suggests new original implementation of adaptive algorithms and thus fosters the performance of embedded accelerators. There were created new operations in the BCE accelerator (UTIA DSP platform); FP Comparator and FP Cumulative Summation. (p. 78).

Generally, the thesis succeeded to achieve their objectives as given on (p. 5) with in detail objective assessment/revision provided on (p.129). In this relation I personally would request more discussion on the possibility for utilization of extended UTIA DSP platform in a Network on Chip (NoC).

The thesis did accomplish its goals and intentions.

d) ***Evaluation of the presented results and their originality***

Some partial results described in the thesis have been accepted for presentation at several prestigious international scientific meetings with strict reviewing processes, among others: 13th ACM International Symposium on Field-Programmable Gate Arrays, Monterey, 2005, DDECS Sopron 2005, ACACES Gent 2005, EFTA Picataway 2006, 21st International Parallel and Distributed Processing Symposium Picataway 2007, International Conference on Field Programmable Logic and Application Delft: IEEE,2007, FPL Amsterdam 2007 and Heidelberg 2008.

On top of author's publications, the list of non-peer reviewed and unpublished works should be taken into account as demonstrator of author's continuous effort of implementation scientific research achievements into recent technologies. Formally: submitted thesis are smoothly structured and written in good English.

Results, as presented and published, clearly proof their high quality and originality.

e) ***What are the merits for practical applications and for further advance of science?***

There are several valuable contributions in between I personally would underline: scientific explanation of the specific adaptive algorithms in relation to the feasibility of their implementation into recent embedded platforms. Simple assessment of those algorithms is presented as supportive tool. Based on this disputation, the HW/SW design has been realized. The promising extension of UTIA DSP platform on the level of basic computing element (BCE) seems to be an enabler for extensive utilization of the platform in most recent application e.g. in robotics sensing, signal filtering or system identification. Massive deployment might be envisioned in this branch.

Despite the current microelectronics provides high performance for successful implementation of even complex algorithms, the limits are still there. As the thesis deals with practical implementation of scientific achievements into real environment, the naturally raised questions are:

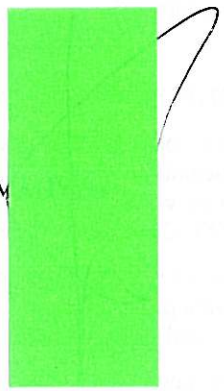
How to assess the limits of current microelectronics in terms of effective implementation of complex algorithms and how such limits shall be shifted by practical utilization of nanotechnologies?

f) ***Can the thesis be classified as an original creative research of its author? Does it include new scientific results published by the author?***

The submitted thesis describes original creative research of its author and it presents valuable scientific results. The chosen topic is systematically treated; it results from extensive amount of preliminary knowledge described in the bibliography. Due to the theoretical complexity of the algorithms it selves and due to the specificity of embedded systems used for their implementation, the reading of the thesis is not easy. To my judgement the results as presented certainly prove high research competence of its author. The thesis meets all requirements expected by the Czech law.

I recommend accepting this thesis for the defence procedure.

Prague, 23th November 2010



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