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Review of Dissertation

The work of Petr Honzik addresses new ways to adapt FPGA behaviour to requirements using self adaptivity. He investigates possible FPGA implementations based on partial dynamic reconfiguration. Since overhead of a hardware implementation is tremendous, the author claims, that state of the art FPGAs are still too small. He implements a simulation instead, demonstrating how future FPGAs could benefit from his ideas.

In chapter 2 a short theory of dynamic reconfiguration is defined. Two types of applications classes are listed, named streaming driven and control dominated. In chapter 3 dynamic reconfigrable devices are listed (Virtex 2-6 and Atmel). Implementation issues for using FPGAs as co-processors are presented. The chapter closes with a comparison of Atmel to Xilinx XC2V1000 devices. Self adaptivity is introduced in chapter 4. Following the authors definition, a self-adaptive system consists of an interface, a reconfigurable computing engine, an observer and a controller. Initial requirements are defined, and an architecture of a self adapting element is introduced, together with first ideas how a basic implementation could looks like.

In chapter 5 various network on chip topologies are compared. A 2D Mesh architecture is selected as underlying communication architecture for this thesis. Placing modules in this 2D Mesh is addressed in chapter 6. Here a "Get Best Node" algorithm is introduced, which is based on a greedy algorithm heuristic. Incremental improvements are shown and simulation results are presented.

The introduction and the background of the work carried out reflects the current state of the art in a very readable manner.

Overall: Only selected benchmarks have been used for comparison of the achieved results. No commercial tools are taken for a direct comparison of the results. Therefore, the industrial relevance of the work is hard to evaluate.

The open problems addressed in the thesis are very important and far beyond of being solved by industrial research, currently. However, real world problems are not solved in the thesis and will not be solvable as long as implementations of these technologies will not fit to the largest available FPGAs.

The topic of the thesis is very relevant for current needs. Dynamic partial reconfiguration will become a more and more important feature. The current market leader Xilinx extends his DPR support. Furthermore, the proposed work is part of the Aether project.

All objective where fulfilled (page 118 ff.)

The methods used have been appropriate. The simulation itself is very nice, and the simulation tool looks good. However, there are some weak points: It looks like nobody has ever tried to map that approach to a real world FPGA. What I really miss is some real measurements on a real FPGA.
I cannot accept the rationale that the FPGAs are still too small. The Xilinx XC2V1000 is outdated, but there are much bigger devices available on the market. Furthermore, DPR is a way to put large netlists on smaller devices. Should that really only run on expensive, huge devices?

I doubt that there is anybody within the Aether-Project who takes care of the implementation, and it remains unclear if there are any implementations within the project which are not part of the thesis. This would at least demonstrate that the simulations are correctly.

The main results are simulation and evaluation of:

- Self Adaptivity
- Network Topologies
- Placement Algorithms
- Dynamic NoC

The work may be important for the Aether-Project and it might help to improve DPR-tools.

The work is creative, but also very straight forward. The network and placement algorithms investigations are new to me.

Here are some drawbacks and possible improvements of the work:

- On page 30 Xilinx Virtex devces are introduced as today's high-end FPGA which is definitely not the case

- Rework of the bibliography is mandatory: Many citations lack of publication information (like Casas et al. 2007, Danek et al .2008, Straka et. al. 2010, and many more)

- Some citations contain typos like
  - Kunle et al. 2008: Design Test of Computers
  - Salminen et al 2007: 10th Euromicro conference on

- CUDA is a programming language which needs to be compiled to a GPU and therefore CUDA Processor is not a known name.

Overall result
I respect the work done so far, however there are some points need to be discussed: I see that the adaptive placement and routing is a very nice algorithm to optimize the placement of units on a given physical network architecture. But does the author really believe that this is the right approach for FPGAs? What is the benefit, when high-end FPGA (see page 30) are not powerful to implement even small applications? Isn't just the overhead by far too high?

I therefore rate the thesis with 2.0 (good). This takes into account, that the simulation is done quite well, and certainly there are applications where the results of this work can help. But it seems to me that FPGAs is just not the right target device to do it this way.

The author of the thesis proved to have an ability to perform research and to achieve scientific results. I do recommend the thesis for presentation with the aim of receiving the degree of Ph.D.

[redacted]

Yours sincerely
Prof. Dr. Udo Kebschull